REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 5, 2002, and the references cited therewith.

Claims 53, 79, 82, 85, 107-112 are amended; as a result, claims 19, 20, 53, 79-87, 98-102, and 104-124 remain pending in this application.

Objections to the Claims

Claims 79, 82, 85, and 107 and 112 were objected to for lack of antecedent basis with respect to the limitation of "the metal layer." The Examiner requested correction of this limitation to "oxide of the metal layer" in claims 79, 82, 85 and 107-110. Likewise, Examiner requested correction of this limitation to "the dielectric layer" in claims 111 and 112.

Though Applicant believes there is adequate antecedent basis for the above-cited claims, Applicant has nevertheless amended the above-cited claims in the manner requested by the Examiner. Applicant therefore respectfully requests that the objection to the above-cited claims be withdrawn.

§102(e) Rejection of the Claims

Claims 19, 53, 79, 81, 85, 87, 107, 111, and 112 were rejected under 35 USC § 102(e) as being anticipated by Azuma et al. (U.S. Patent No. 5,708,302) (hereinafter, "Azuma").

Applicant does not admit that Azuma is prior art under 35 USC § 102(e), and reserves the right to swear behind this reference. However, Applicant nevertheless believes that Azuma is distinguishable from Applicant's claimed invention, as discussed below.

Claim 53 has been amended to eliminate the so-called "product by process" limitation of "formed by oxidizing a metal layer..." The limitation now reads "...that includes an oxide of a metal layer..." Accordingly, claim 53 now includes the same limitation relating to the dielectric layer as in the other claims cited above.

The Examiner states in the Office Action on page 5, second paragraph, that (emphasis added):

> Azuma et al. discloses a capacitor (Fig 1) comprising a first conductive capacitor plate 34 formed of a first material; a second conductive capacitor plate 28; and a dielectric layer 26 interposed between said first and second conductive capacitor plates, <u>wherein said dielectric is a metal oxide overlaying the first conductive capacitor plate</u>.

However, Applicant's claimed invention does not merely include a metal oxide dielectric between the first and second conductive capacitor plates. Rather, Applicant's claimed invention includes the limitation that the ***dielectric be an oxide of a metal layer overlying the first conductive capacitor plate***.

Azuma does not include this limitation. As described in great detail in Azuma (see, e.g., the flow diagram of FIG. 3 and the discussion in column 7, line 51 to col. 7, line 56; also, col. 9, line 21 to col. 10, line 8) the metal oxide layer (26) is formed using specially formulated "liquid precursor" containing various metal compounds. The liquid precursor is designed to form a perovskite or a perovskite-like layered superlattice and so its formation is rather involved. Col. 2, line 65 to col. 3, line 45. The liquid precursor is then spun onto the surface of the bottom electrode. The liquid precursor is then dried and annealed. Col. 10, lines 3-4. The thickness of the film is then measured to see if it has the desired thickness. If the thickness is not as desired, the steps are repeated (see flow diagram of FIG. 3, steps P72 through P76). The metals in the metal oxide layer are therefore added to the device via a series of complex steps.

In contrast, in Applicant's claimed invention, the metal used in forming the dielectric layer is provided by a metal layer overlying the first conductive capacitor plate. In other words, the metal forming the dielectric layer is provided by a portion of the capacitor device itself. Oxidization of the metal layer overlying the capacitor plate is a far simpler way of forming the dielectric than using all of complex method steps of Azuma.

In view of the above, Applicant respectfully submits the above-cited claims are not anticipated by Azuma because Azuma does not include all of the claim elements of Applicant's invention, most notably the limitation involving forming the dielectric layer as an oxide of a metal layer overlying the first conductive capacitor plate. Applicant therefore respectfully

requests withdrawal of the rejection of the above-cited claims and allowance of same.

§103 Rejection of the Claims

Claims 20, 82, 84, 109, and 110 were rejected under 35 USC § 103(a) as being unpatentable over Blodgett et al. (U.S. Patent No. 5,811,990) (hereinafter, "Blodgett") in view of Azuma.

The obviousness rejection of system claims 20, 82, 84, 109 and 110 is based on the assumption that Azuma anticipates the portion of these claims that recite the capacitor structure. However, as discussed immediately above, Applicant respectfully submits that Azuma does not anticipate Applicant's claimed capacitor structure because Azuma does not teach, suggest or motivate the limitation that the dielectric layer be an oxide of a metal layer overlying the first conductive capacitor plate.

Applicant therefore respectfully requests that the obviousness rejection be withdrawn and the above-cited claims allowed.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney, Joe Gortych, at (802) 660-7199 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 3 day of September, 2002.

Tina Kohout
Name

[signature]
Signature

Docket No. 303.455US3 Micron Ref. No. 95-0505.02
WD # 353042

CLEAN VERSION OF PENDING CLAIMS

DEVICES HAVING IMPROVED CAPACITANCE AND METHODS OF THEIR FABRICATION
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Claims 19, 20, 53, 79-87, 98-102, and 104-124, as of September 3, 2002 (Date of Response to First Office Action after CPA).

19. A capacitor, comprising:

a first conductive capacitor plate of a first material;

a second conductive capacitor plate; and

a dielectric interposed between said first and second conductive capacitor plates, wherein said dielectric is an oxide of a metal layer of a second material overlying the first conductive capacitor plate.

20. A memory system, comprising:

a monolithic memory device, comprising a capacitor, wherein the capacitor comprises:

a first conductive capacitor plate;

a second conductive capacitor plate; and

a dielectric interposed between said first and second conductive capacitor plates, wherein said dielectric is an oxide of a metal layer overlying the first conductive capacitor plate; and

a processor configured to access the monolithic memory device.

Sub F2 E1

53. (Amended) A capacitor comprising:

a first capacitor electrode;

a dielectric layer that includes an oxide of a metal layer overlying the first capacitor electrode; and

a second capacitor electrode.

Sub F3 E2

79. (Amended) The capacitor of claim 19, wherein the oxide of the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

80. The capacitor of claim 79, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

81. The capacitor of claim 19, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

Sub F4

E3

82. (Amended) The memory system of claim 20, wherein the oxide of the metal layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

83. The memory system of claim 82, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

84. The memory system of claim 20, wherein the second conductive capacitor plate is formed from a material selected from the group consisting of polysilicon and metal.

Sub F5

E4

85. (Amended) The capacitor of claim 53, wherein the dielectric layer is formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel.

86. The capacitor of claim 85, wherein the at least one metal is alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

87. The capacitor of claim 53, wherein the second capacitor electrode is formed from a material selected from the group consisting of polysilicon and metal.

98. A capacitor formed by a process comprising:

forming an insulative layer overlying a substrate;

masking the insulative layer to define a region in which to fabricate the capacitor;

removing the insulative layer in an unmasked region to expose a portion of the substrate;

depositing a polysilicon layer overlying the insulative layer and the substrate and contacting the substrate;

removing portions of the polysilicon layer to expose an upper surface of the insulative layer;

depositing a metal layer to overly the polysilicon layer, the metal layer being formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead;

contacting the metal layer with an electrolytic solution;

applying an electrical potential to the electrolytic solution and the metal layer;

oxidizing at least a portion of the metal layer to form a metal oxide to function as a dielectric layer; and

forming an electrically conductive layer overlying the metal oxide.

99. The capacitor of claim 98, wherein the electrolytic solution is a basic solution.

100. The capacitor of claim 98, wherein the electrolytic solution is an acidic solution.

101. The capacitor of claim 98, wherein the electrolytic solution is a solution of one part NH_4OH to ten parts water.

102. The capacitor of claim 98, wherein the electrolytic solution is a 0.1 molar solution of $HClO_4$.

104. A capacitor, comprising:

a first conductive plate serving as a first electrode of the capacitor;

a second conductive plate serving as a second electrode of the capacitor, the second conductive plate formed from a material selected from the group consisting of polysilicon and metal; and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead.

105. A memory system, comprising:

a monolithic memory device comprising a capacitor, wherein the capacitor comprises

a first conductive capacitor plate,

a second conductive capacitor plate formed from a material selected from the group consisting of polysilicon and metal, and

a dielectric interposed between the first and second conductive plates, wherein the dielectric is an oxide of a metal layer overlying the first conductive plate, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a processor configured to access the monolithic memory device.

106. A capacitor comprising:

a first capacitor electrode comprising polysilicon;

a dielectric layer formed by oxidizing a metal layer overlying the first capacitor electrode, the metal layer formed from at least one metal selected from the group consisting of titanium, copper, gold, tungsten, and nickel, alloyed with at least one additional metal selected from the group consisting of strontium, barium, and lead; and

a second capacitor electrode formed from a material selected from the group consisting of polysilicon and metal.

Sub F6

107. (Amended) The capacitor of claim 19, wherein the oxide of the metal layer comprises titanium.

108. (Amended) The capacitor of claim 19, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the oxide of the metal layer.

E5

109. (Amended) The memory system of claim 20, wherein the oxide of the metal layer comprises titanium.

110. (Amended) The memory system of claim 20, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the oxide of the metal layer.

111. (Amended) The capacitor of claim 53, wherein the dielectric layer comprises titanium.

112. (Amended) The capacitor of claim 53, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and

E5

the dielectric layer.

113. The capacitor of claim 104, wherein the first conductive plate comprises polysilicon having a thickness of 200 to 400 Angstroms.

114. The capacitor of claim 104, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

115. The memory system of claim 105, wherein the first conductive capacitor plate comprises polysilicon.

116. The memory system of claim 105, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first conductive plate and the metal layer.

117. The capacitor of claim 106, wherein the first capacitor electrode has a thickness from 200 to 400 Angstroms.

118. The capacitor of claim 106, further comprising at least one of a diffusion barrier layer and an oxidation resistant layer interposed between the first capacitor electrode and the metal layer.

119. A capacitor structure formed on a substrate, comprising:

a first conductive capacitor plate formed atop the substrate;

a first metal layer formed atop the first conductive capacitor plate;

a first metal oxide layer formed from the metal layer such that the remaining first metal layer forms part of the first conductive capacitor plate; and

a second conductive layer formed atop the first metal oxide layer.

120. The capacitor structure of claim 119, further including:

a second metal layer formed atop the second conductive layer;

a second metal oxide layer formed from the second metal layer such that the remaining second metal layer forms part of the second conductive layer;

a third conductive layer formed atop the second metal oxide layer, wherein the first and second metal oxide layers and the second conductive layer form the dielectric of the capacitor and the third conductive layer serves as a second conductive capacitor plate.

121. The capacitor structure of claim 119, wherein:

the first conductive capacitor plate comprises polysilicon and the first metal layer comprises a metal selected from the group of metals consisting of titanium, tungsten, copper, gold, and nickel.

122. The capacitor of claim 119, wherein the first metal layer is substantially completely oxidized to form the metal oxide layer.

123. The capacitor of claim 119, wherein the first metal oxide layer has a thickness of between 10 and 1000 Angstroms.

124. The capacitor of claim 119, wherein the first metal layer is alloyed with another material.